## Applicant(s)/Patent Under Reexamination Application/Control No. 10/632,930 FUKUNAGA, TAKESHI Notice of References Cited Examiner Art Unit Page 1 of 1 William M. Brewster 2823

## **U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
X	A	us-6,682,761 Bl	98-298	FUKUNAGA	438/459
	B	US-			
	C	US-			
	Q	US-			
	Ε	US-			
	F	US-			
	G	US-			
	н	US-			
	ì	us-			
	J	US-			
	к	US-			
	٦	US-			
	М	US-		,	·

## FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	P					
	ø					
	R					
	s					
	Ŧ					

## NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	บ	Stanley Wolf Ph.D. In Silicon Processing for the VLSI Era, Volume 2: Process Integration, Lattice Press, 1990, pp. 238-9.				
	٧	·				
	8					
	x					

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office PTO-892 (Rev. 01-2001)